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A REVIEW PAPER ON IMPROVED PERFORMANCE OF STATIC RANDOM ACCESS MEMORY BASED ON LOW POWER CONSUMPTION

Naresh Kumar Gedam *[1], Prof. Rajeev Thakur [2]
Department of Electronic Communication, NIST, Bhopal, India
[1]nrsh.gdm@gmail.com, [2]rajeev.thakur@nrigroupindia.com

Abstract: *The need for low power integrated circuits is well known because of their extensive use in the portable electronic equipments. On-chip SRAMs (Static Random Access Memory) determine the power dissipation of SoCs (System on Chips) in addition to its speed of operation. Hence it is essential to have energy-efficient SRAMs—Static Random Access Memories (SRAMs) which focuses on optimizing delay and power. Static Random Access Memory (SRAM) continues to be a critical component across a wide range of microelectronics applications from consumer wireless to high-performance processors, multimedia and System on Chip (SoC) applications, the leakage power of Static Random Access Memory (SRAM) is becoming one of the most critical concerns for low power applications and CMOS SRAM cell consumes very less energy and have less read and write time. In a review on 6T SRAM cell, 9T SRAM cell, 10T SRAM cell configurations are compared to our proposed SRAM circuit based on low power consumption. This learning paper plans to provide an Energy Efficient Low Power SRAM Cell, and here various techniques and approaches are discussed to achieve better performance.*

Keywords: SRAM, Low Power Consumption, Energy Efficient, Delay Write, Delay Read, Six Transistors.

I. INTRODUCTION

Low power SRAMs have become a critical component of many VLSI chips. This is especially true for microprocessors, where the on-chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processor and the main memory. Due to the increased integration and operating speeds, power dissipation has become an important consideration both as well as due to the explosive growth of battery-operated appliances [1]. There are two purposes of an SRAM (Static Random Access Memory) design: First is to provide a direct interface with the CPU at speeds not attainable by DRAMs, and second is to replace DRAMs in systems that require shallow power consumption. In the first role, the SRAM serves as cache memory, interfacing between DRAMs and the CPU. The other driving force for SRAM technology is low power applications [2]. Research on very low threshold voltage and ultra-thin gate oxide is in a progressive stage due to a reduction in the threshold voltage and the gate oxide thickness. The phenomena like intrinsic parameter fluctuation, random dopant fluctuation, oxides thickness fluctuation, and line edge roughness further degrade the stability of SRAM cells. Large scale integration and fabrication process have resulted in increased density of devices by decreasing the physical device dimensions. Performance in terms of low power dissipation and high-speed operation are the significant challenges of integrated circuit design in deep submicron and nanoscale technologies. Designing a high-performance VLSI chip is becoming a necessity for mobile communication and computing devices. Static Random Access Memories (SRAM) is read/write memory devices that can read data from or write data to any of its memory addresses. Static random access memories (SRAM) store data in flip-flops, which retain data as long as the SRAM is powered up. In SRAM, there are four transistors for storing bit that form two cross-coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional access transistors serve to control the access to a storage cell during read and write operations. [3].two types of memory. Dynamic Random Access Memory (DRAM) devices are used in a wide range of electronics applications. Although they are produced in many sizes and sold in a variety of packages, their overall operation is essentially the same. DRAMs are designed for the sole purpose of storing data. The only valid services on a memory device are reading the data stored in the device, writing (or saving) data in the device, and refreshing the data periodically. To improve efficiency and speed, several methods for reading and writing the memory have been developed. Dynamic random access memory (DRAM) integrated circuits (ICs) have existed for more than twenty-five years. DRAMs evolved from the earliest 1-kilobit (Kb) generation to the recent 1-gigabit (Gb) generation through advances in both semiconductor process and circuit design technology. Tremendous advances in process technology have dramatically reduced feature size, permitting ever-higher levels of integration. These increases in combination have been accompanied by significant improvements in component yield to ensure that overall process solutions remain cost-effective and competitive Technology improvements; however, are not limited to semiconductor processing. Many of the advances in process technology have been accompanied or enabled by advances in circuit design technology. DRAM stores a bit of data using a transistor and capacitor pair, which together comprise a Dynamic RAM memory cell. The capacitor holds a high/low charge, and the transistor acts as a switch that lets the control circuitry on the chip read the capacitor's state of charge or changes it. This form of memory is less expensive to produce than static RAM; eventually, it is the predominant form of computer

memory used in modern computers. Dynamic RAM is considered volatile, as it lost the information or data when power is removed from the system [4].

SRAM: Static Random Access Memory (SRAM) to be one of the most fundamental and vitally essential memory technologies today. Because they are fast, robust, and easily manufactured in standard logic processes, they are nearly universally found on the same die with microcontrollers and microprocessors. Due to their higher speed, SRAM based Cache memories and System-on-chips are commonly used. Due to device scaling, there are several design challenges for nanometer SRAM design. Low power SRAM design is crucial since it takes a significant fraction of the total power and die area in high-performance processors. An SRAM cell must meet the requirements for the operation in submicron/nano ranges. The scaling of CMOS technology has significant impacts on SRAM cell random fluctuation of electrical characteristics, and substantial leakage current the density of static random access memory (SRAM) has tremendously increased in recent years due to the requirement of a large number of memories in a system on chip (SoC). The current improvement of fabrication technology also realizes the smaller size of the SRAM cell. This new Cell consumes less power during operation. Also, it can be operated at lower supply voltage. However, the stability of the SRAM cell is severely affected by the decrease in supply voltage [4]. The Cell becomes more vulnerable to noise and radiation at low voltage, so maintaining an acceptable SNM is becoming challenging. SRAM is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static RAM differentiates it from dynamic RAM, which must be periodically refreshed. Static RAM exhibits data remanence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. The SRAM cell has three different states, such as standby, reading, and writing. To operate in read mode and write mode, SRAM should have "readability and "write stability," respectively. Static RAM Cell Design: Static RAM is an essential class of memory. It consists of two cross-coupled inverters, which form positive feedback with two possible states illustrated in figure 2 given below.

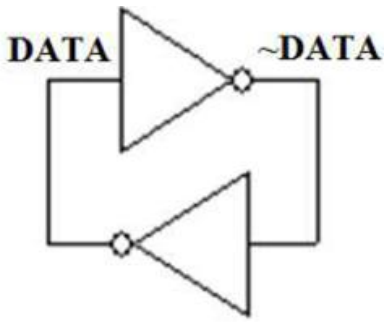

Figure 1. Static RAM Cell

A. Standby: If the word line is not asserted, the access transistor m5 and m6 disconnected the Cell from the bit line [9]. The two cross-coupled inverters formed, and it will continue to reinforce each other as long as they are connected to the supply.

B. Reading: Let as consider 6T SRAM cell shown in figure.1. Assume that the content of the memory is 1, stored at Q. The read cycle is started by pre-charging both the bit lines to a logic 1, then asserting the word line (WL), enabling both the access transistors m5 and m6 and then the second step occurs when the values stored in Q and Qbar are transferred to the bit lines by leaving BL at its pre-charged value and discharging BL through m1 and m5 to a logic 0.

C. Writing: The write cycle begins by applying the value to be written to the bit lines. If we wish to write a **0**, we will use a **0** to the bit lines, i.e., setting BL to **1** and BL to **0**. This is similar to using a reset pulse to an SR-latch, which causes the flip flop to change state. A **1** is written by inverting the values of the bit lines. WL is then asserted, and the value that is to be stored is latched in. This works because the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the Cell itself so they can easily override the previous state of the cross-coupled inverters. In practice, access NMOS transistors M_5 and M_6 have to be stronger than either bottom NMOS (M_1, M_3) or top PMOS (M_2, M_4) transistors. This is easily obtained as PMOS transistors are much weaker than NMOS when same sized. Consequently, when one transistor pair (e.g., M_3 and M_4) is only slightly overridden by the writing process, the opposite transistors pair (M_1 and M_2) gate voltage is also changed. This means that the M_1 and M_2transistors can be easier overridden, and so on. Thus, cross-coupled inverters magnify the writing process [5].

Transistor Memory Cells (6T): Memory Architecture is Random-access architecture, which is an Asynchronous design. The name is derived from the fact that memory locations (addresses) can be accessed in random order at a fixed rate, independent of physical location, for reading or writing. The storage array, or core, is made up of simple cell circuits arranged to share connections in horizontal rows and vertical columns. The horizontal lines, which are driven only from outside the storage array, are called word lines, while the vertical lines, along with which data flows into and out of cells, are called bit lines. A cell is accessed for reading or writing by selecting its row and column. Each Cell can store 0 or 1. Fig 3 shows the conventional SRAM cell. Word line is used for enabling the access transistors N1 and N4 for a write operation. BL and ~BL lines are used to store the data and its complement. Both the bit lines (BL and ~BL) are used to transfer the data during the read and write operations in a differential manner. To have a better noise margin, the data signal and its inverse are provided

to BL and ~BL, respectively. For a write operation, one BL is High, and the other bit line remains in low condition. The memory cell has shown the basis for most static random-access memories in CMOS technology [6].

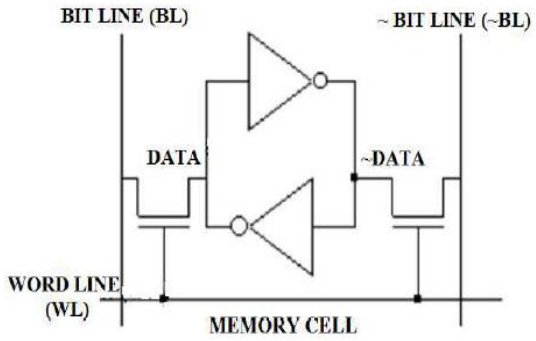

Figure 2. Basis static random-access memories.

It uses six transistors in figure3 to store and access one bit. The four transistors in the centre form two cross-coupled inverters. It has 2 pull up PMOS, and 2 NMOS pull-down transistors as two cross-coupled inverters and two 2 NMOS access transistors to access the SRAM cell during Read and Write operations. In actual devices, these transistors are made as small as possible to save chip-area and are very weak. Due to the feedback structure, a low input value on the first inverter will generate a high value on the second inverter, which amplifies (and stores) the low value on the second inverter. Similarly, a high input value on the first inverter will generate a low input value on the second inverter, which feeds back the low input value onto the first inverter. Therefore, the two inverters will store their current logical value, whatever value that is [7].

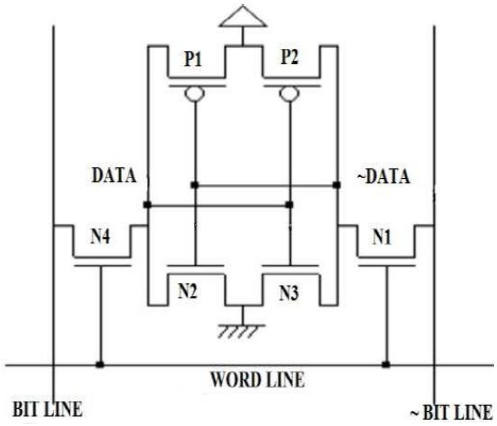

Figure 3. Conventional 6T SRAM Cell

II. LITERATURE SURVEY

Rahman et al. [8]. Read stability is one of the most important factors for designing efficient SRAM cells. This research presents an in-depth understanding of 6T-SRAM cell's functionality and comparative performance study of the bit-cell under three different technology nodes of 32nm, 22nm, and 16nm. Measures are taken to mitigate the effect of a drastic reduction in Read-Static-Noise- Margin at 16nm CMOS technology by implementing the 8TSRAM structure. To design an SRAM cell, in the present research, read and hold stability are taken into consideration. Then static noise margins are estimated for hold and read operations by meticulously selecting the cell-parameters. The cell ratio has highly impacted on the operation of the memory cell. Temperature dependence is also analyzed for 6T and 8T Cells at 16nm technology. HSPICE simulation software is employed, and a set of transistors incorporating high-k/metal gate from PTM high-performance models are used in this research.

Kim TH et al. [9]. Proposes 6T and Figure4 shows the circuit diagram of a conventional SRAM cell. Before the read operation begins, the bit line (BL) and bit bar line (BLB) is pre-charged to as high as supply voltage Vdd. When the word line (WL) is selected, the access transistors are turned on. This will cause a current to flow from the supply voltage (Vdd) through the pull-up transistor TP1 of the node storing ''1''. On the other side, the current will flow from the pre-charged bit bar line to ground, thus discharging a bit bar line. Thus, a differential voltage develops between the BL and BL. This small potential difference between the bit lines is sensed and amplified by the sense amplifiers at the data output.

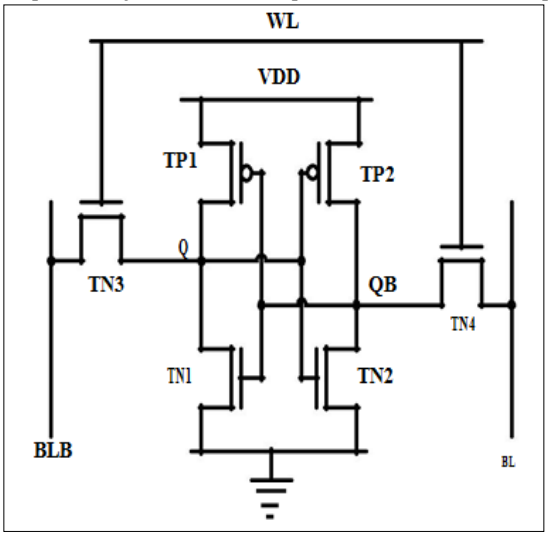

Figure 4. 6T SRAM

S. Dasgupta et al. [10] analyzed the performance parameters of SRAM in three different formats of 6T, 8T, and 9T Cells at 90nm technology. Their analysis incorporates data access delays, noise margins, and sub-threshold leakage for each format. But the overall read time estimation was not explained. Also, no data of power consumption for read operation was presented. However, in this paper we proposed a specific technique to measure the read time. Also, estimation of power consumption is demonstrated for both standby and read mode of the SRAM cell. Then to overcome the Read-Static-Noise-Margin problem of 6T Cell at 16nm technology, we redesigned it in 8T cell format.

A. Singh et al. [11]. Analyzed the design of 8T SRAM using energy recovery logic, and by using the energy recovery logic cell stability, leakage noise has been improved. Figure 8 shows the 8T SRAM using energy recovery logic. The proposed SRAM is structurally close to the conventional CMOS SRAM. The PMOS transistor connected between the power line and Vdd and NMOS is connected to GND and Vdd. The energy recovery signal is input from the bit line. While the input voltage increases, the other voltage depends on the circuit.

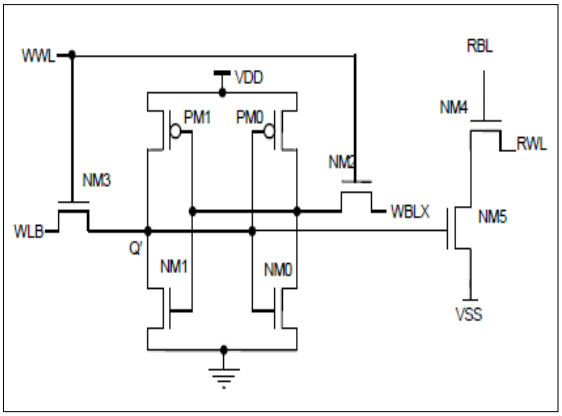

Figure5. 8T SRAM cell

Tajalli et al. [12]. Proposed subthreshold SCL (source coupled logic) for low power SRAM and low activity rate digital systems. The subthreshold leakage consumption of conventional CMOS circuits is more pronounced subthreshold SCL can be used effectively for reducing the power consumption. A 9T memory cell has been developed to reduce the standby current while the SRAM array is operating at 2.1MHz clock frequency. The proposed 9T memory cell is shown in figure 4. The power consumption of the proposed circuit style is maintained in nanometer CMOS technology nodes.

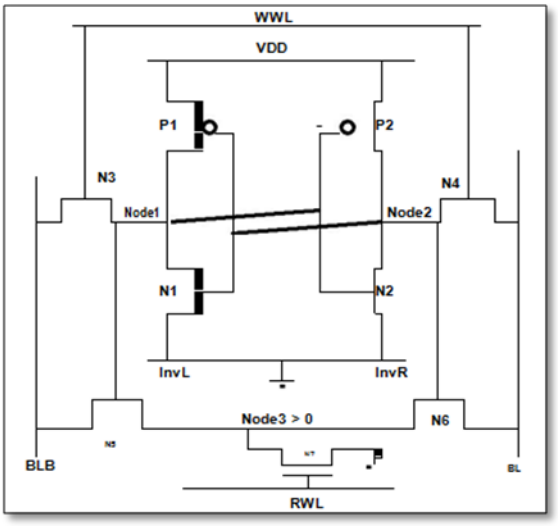

Figure 6. 9T SRAM Cell

A. Priyadarshini et al. [13]. Proposed low power CMOS Static Random Access Memory based field programmable gate arrays architecture and analyzed CMOS SRAMs that are used for on-chip reconfiguration. This architecture is based on CMOS logic. Fast and low power SRAM based on 10T SRAM cells is shown in figure 6. Compared to conventional 4T and 6T SRAM cells delay is improved and the time for pre-charged is reduced, 10T SRAM design avoids high switching activities on memory read bit lines and thus saves most of the charge or pre-charge power.

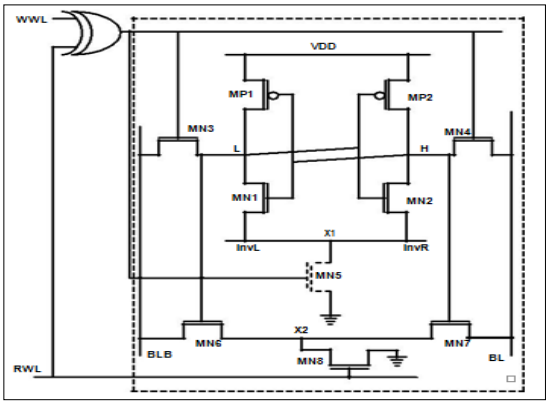

Figure 7. 10T SRAM

III. EXPECT OUTCOME

The main aim of this paper is to reduce power consumption in the SRAM cell. Provide an energy-efficient SRAM Cell, and here various techniques and approaches are discussed to achieve better performance and low power consumption, how many transistors are used in the implementation of SRAM.

IV. CONCLUSION

Different SRAM configurations: 6T and 9T have been studied for their performance analysis. Literature survey reveals that 6T SRAM cell has the advantage of higher noise margin and smaller power dissipation in comparison with other discussed SRAM configurations. The studied results also show that this SRAM cell has the least power delay product among different SRAM configurations (6Tand 9T SRAM configurations) in 90nm CMOS technology. These designs are well preferred for various low power applications. Various techniques to reduce power dissipation have been developed, and it can be used for low power and high-speed applications. The micro-wind program allows the designer to design and simulate an integrated circuit at the physical description level. Energy efficiency and leakage are the main concerns in the SRAM. The remedies to overcome this problem are discussed in this survey with various approaches and design techniques where they have undertaken. I am going to implement a modified 8T SRAM with the Self-Adaptive Voltage Level circuit to minimize leakage and to improved energy efficiency.

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